Total ionizing dose effects on I-V and noise characteristics of MOS transistors in a 0.18 m CMOS Image Sensor process

Conference or Workshop Item

Total Ionizing Dose Effects on I-V and Noise Characteristics of MOS Transistors in a 0.18 μm CMOS Image Sensor Process

Thomas Greig, Konstantin Stefanov, Andrew Holland, Andrew Clarke, David Burt and Jason Gow

***Abstract*— This paper presents an investigation into total ionizing dose (TID) effects on I-V and noise characteristics of MOS transistors manufactured in a 0.18 μm CMOS Image Sensor (CIS) process. The CIS are intended for use in space science missions experiencing harsh radiation environments, such as ESA's forthcoming JUICE mission. Devices were therefore irradiated to various TID levels up to 1 Mrad. Following irradiation, significant leakage current and threshold voltage modification was observed, and this was found to be more severe for devices with small channel geometries. Noise spectral density measurements were also performed at the different irradiation steps. Noise in the smaller geometry devices was found to increase following irradiation, whereas for larger devices it was not significantly affected. These findings enable future assessment of the effects of TID on functional and electro-optical characteristics of high performance CIS designs for use in space.**

***Index Terms*—CMOS image sensor (CIS), metal oxide semiconductor (MOS) transistor, total ionizing dose (TID).**

I. Introduction

A. Requirement for CMOS Image Sensors in Space

Major space missions establish large programmes to investigate radiation effects in image sensors (Euclid, Gaia, Hubble, etc) and the impact on performance. Effects can be transient and instantaneous, or can accumulate over time due to total ionizing dose (TID) and displacement damage (DD). As missions travel to more hostile areas of the Solar System, the damage experienced by components is expected to be too harsh for optimal operation of the existing charge-coupled device (CCD) technology. As an example, the total ionizing dose experienced over the lifetime of the planned ESA JUICE mission [1] is estimated at 500 krad(Si).

B. Perceived CIS Radiation Tolerance

A major inherent advantage of CMOS image sensors (CIS) is that, unlike CCDs [2], they do not suffer charge transfer problems induced by DD and are theoretically less susceptible to various TID induced effects due to the use of thinner gate oxide layers in modern CMOS manufacturing processes [3]. CIS are therefore being explored for missions such as JUICE and others.

C. Total Ionizing Dose Effects in MOS Transistors

MOS transistors are the building blocks at the heart of all CMOS image sensors. Unlike CCD pixels, which only consist of MOS capacitors and no active components, each CIS pixel normally contains at least three MOS transistors and a photodiode. The peripheral circuitry also consists of many thousands of transistors used to read out the pixel array [4]. Characterisation of the effects of radiation damage on the behaviour of the various transistors in the signal processing chain is important to isolate the causes of any problems and mitigate them through modifications to the design or operational conditions.

The individual or collective behaviour of MOS transistors is generally simulated using models supplied by the wafer foundry. Such models are critical to designing large scale integrated circuits. It is rare for CIS designers to physically characterise the behaviour of individual transistors. Physical characterisation normally focuses on the collective behaviour of the final built device. Such an approach is not ideal when constructing complex mixed signal integrated circuits such as CMOS image sensors, especially those which will be subjected to harsh radiation environments. Radiation damage can cause the device behaviour to deviate from the modelled performance specified by the wafer foundry, leading to unexpected effects. It is therefore very important to understand the effects at the single transistor level.

There are basically two effects of radiation on MOS transistors. The first is due to the ionizing effects of radiation interacting within SiO_2 regions present in the device [5]. The interactions can lead to trapped positive charge and also increase the defect density at Si-SiO_2 boundaries (also known as interface states). These types of damage are generally collectively referred to as surface damage. The second is displacement damage within the bulk silicon which causes the transfer problems in CCDs [2] but has little effect on transistor characteristics.

Modern CMOS transistors have two main oxide regions, as

This work was funded by the United Kingdom Space Agency (UKSA), e2v and the Open University.

T. Greig, K. Stefanov, A. Holland, A. Clarke and J. Gow are with the Centre for Electronic Imaging, the Open University, Walton Hall, Milton Keynes, MK7 6AA, United Kingdom. (e-mail: Thomas.Greig@open.ac.uk; Konstantin.Stefanov@open.ac.uk; Andrew.Holland@open.ac.uk; Andrew.Clarke@open.ac.uk; Jason.Gow@open.ac.uk).

D. Burt is with e2v Ltd, 106 Waterhouse Lane, Chelmsford, Essex, CM1 2QU, United Kingdom (e-mail: David.Burt@e2v.com).

shown in Fig. 1. The gate oxide is used to form the channel, and the shallow trench isolation (STI) oxide is used to isolate adjacent transistors from one another. In comparison with current CCDs, CMOS transistors are less susceptible to charge trapping in the gate oxide as it is normally very thin (<10 nm). More of a problem is the STI which is significantly thicker (~300 nm) and the charge trapping is proportionately more severe, leading to parasitic leakage currents. The effect of increased defect density (interface states) at oxide boundaries is an issue for both types of region and will lead to increased noise.

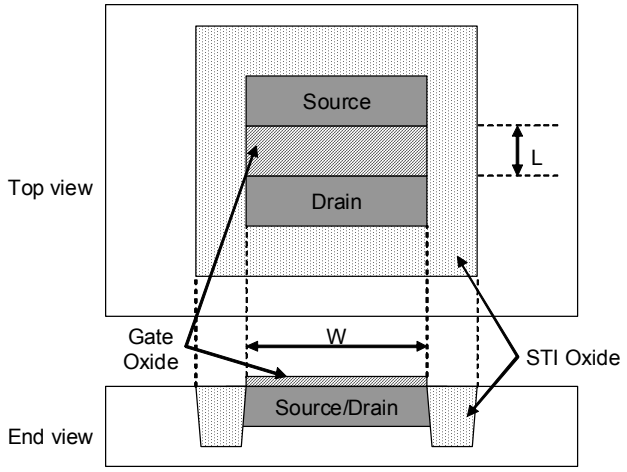

Fig. 1. Simplified top view and cross section of a modern MOS transistor showing the two main oxide regions prone to radiation damage effects

II. Experimental Details

A. Test Structures Description

A variety of NMOS and PMOS test transistors were designed by e2v and fabricated by TowerJazz Semiconductor using a 0.18 µm CIS process. The transistor design parameters are summarized in Table I. Devices with a range of channel geometries between 0.42 µm and 10.00 µm were implemented. All transistors shared a common gate connection with all NMOS source connections connected to the substrate and all PMOS source connections connected to the N-Well. Drain connections were separate for each transistor. All pins were protected by ESD protection diodes with reverse leakage current of 80 pA (20 °C).

TABLE I
SUMMARY OF TEST TRANSISTOR PROPERTIES

Name	Type	Typical V_T (V)	Width (µm)	Length (µm)
M2	NMOS	0.7	0.42	0.42
M54	NMOS	0.7	1.60	0.80
M1	NMOS	0.7	4.00	2.00
M52	NMOS	0.7	10.00	10.00
M53	NMOS	0.7	5.00	1.00
M49	PMOS	0.7	10.00	10.00
M51	PMOS	0.7	0.42	0.42

B. Irradiation Configuration

All devices were irradiated at AMEC's cobalt-60 gamma irradiation facility on the MRC Harwell site in the UK. I-V and noise characteristics were measured before and after each irradiation step (further experimental details of the I-V and noise measurements are given in the relevant results section). The irradiations were performed at room temperature and were divided into two phases. In the first phase devices were irradiated unbiased for a range of doses between 0 and 500 krad, at a dose rate of 10 krad/hr. In the second phase devices were irradiated biased (V_{GS} = 1.2V, V_{DS} = 2.4V) to 0, 500 krad and 1 Mrad, at a dose rate of 7 krad/hr. A data logger was used to regularly monitor and verify bias levels were correct during the irradiations.

III. Results and Discussion

A. I-V Measurements

1) Experimental Setup

I-V characteristics of each device were measured before and after each irradiation using two computer-controlled Keithley 2400 SourceMeters capable of measuring currents greater than 10 pA. I-V characteristics were measured by sweeping the gate or drain voltage.

2) Unbiased Irradiation Results

Fig. 2 shows the drain current (I_{DS}) characteristics as a function of gate-source voltage (V_{GS}) for the smallest NMOS transistor (M2, 0.42 µm × 0.42 µm) before irradiation and after exposure to a TID of 500 krad. The characteristics are shown on a linear plot and semi-log plot to highlight the sub threshold voltage conduction characteristics. Little or no change was observed within the measurement limitations. Similar observations were made for the range of transistor geometries therefore no further measurements of devices unbiased during irradiation are presented here. It should however be noted that the current measurement resolution is thought to be too coarse to measure the small changes in leakage current for un-biased irradiations. For the above reasons this paper focuses on the variation in I-V characteristics seen for the biased irradiations.

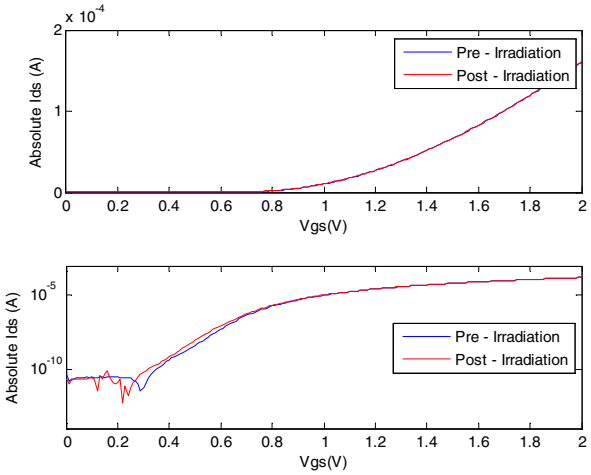

Fig. 2. Drain current characteristics for transistor M2 before irradiation and after 500 krad. V_{DS} = 3 V.

3) Biased Irradiation Results

For the biased irradiations, 10 transistors of each type were

characterised pre-irradiation and after cumulative doses of 500 krad and 1 Mrad. This was primarily to improve the noise investigation described later. Fig. 3 shows the mean drain current characteristics (across ten devices) as a function of gate-source voltage for the smallest NMOS transistor design (M2, 0.42 µm × 0.42 µm), after each irradiation step. A significant increase in drain current for a given gate-source voltage was observed following the first 500 krad irradiation. The drain leakage current (V_{GS} = 0V) is in the range 10-20 nA. Following the second 500 krad irradiation relatively little change in the characteristics was observed. The mean drain characteristics for the smallest PMOS transistor are shown in Fig. 4. A slight overall shift was observed, but no significant change in leakage current (V_{GS} = 0V) was seen. No overall shift or change in leakage current was observed in the largest PMOS transistor.

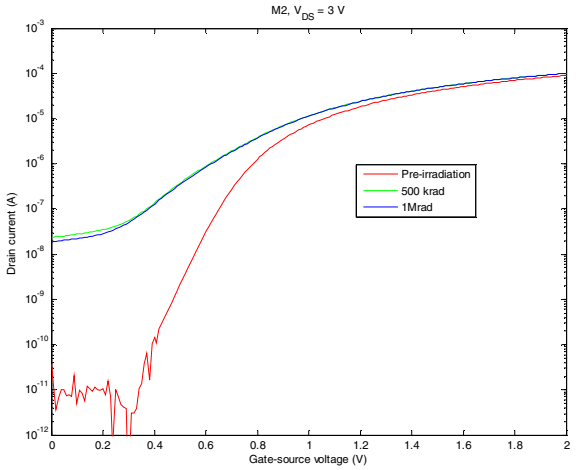

Fig. 3. I_{DS} vs. V_{GS} characteristics for smallest NMOS transistor (M2, 0.42 µm × 0.42 µm) before irradiation and after 500 krad and 1Mrad TID (V_{DS} = 3V).

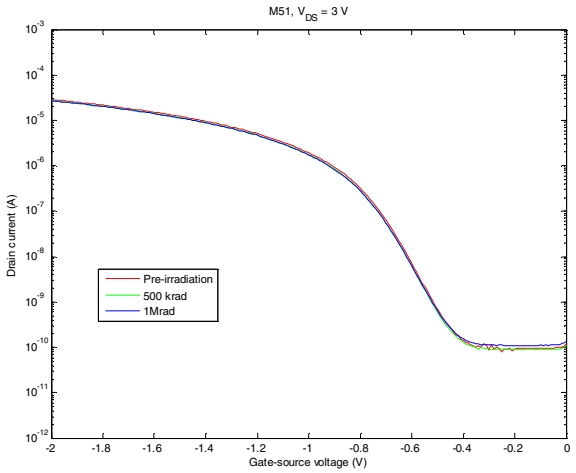

Fig. 4. I_{DS} vs. V_{GS} characteristics for smallest PMOS transistor (M51, 0.42 µm × 0.42 µm) before irradiation and after 500 krad and 1 Mrad TID (V_{DS} = -3V).

The mean leakage current (V_{GS} = 0V) variation with TID was calculated for each transistor type. The results for all NMOS devices are shown in Fig. 5. It can be seen that the leakage current increased significantly after the first 500 krad irradiation but no further increase was seen following the second 500 krad. The largest increase was seen for the smallest transistor and the increase appeared to reduce as the channel length was increased, with the exception that M1 (4.00 µm × 2.00 µm) showed the smallest leakage. No change with dose was observed for the PMOS devices (not shown).

The threshold voltage variation with TID was estimated by extracting the gate-source voltage required to maintain a drain current of 10 µA, for each device at each TID. The shift relative to the pre-irradiation values as a function of dose for each NMOS device is shown in Fig. 6. In all cases a negative shift is seen after the first 500 krad with no further shift after the second 500 krad. The magnitude of the shift increases as the channel length reduces. The shift was also estimated for the PMOS devices and was found to be much less (~ 10 mV).

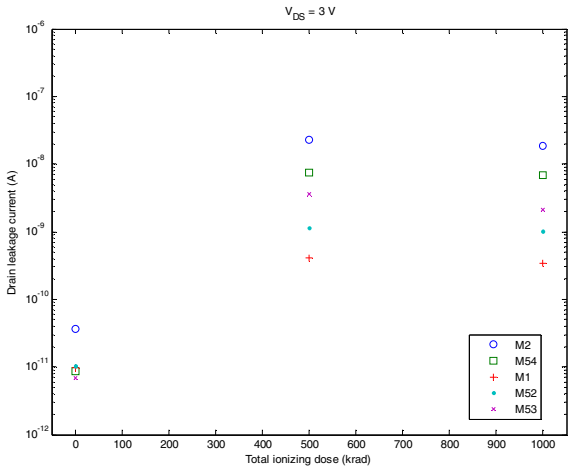

Fig. 5. Drain leakage current (V_{GS} = 0V) variation with TID for all NMOS transistor geometries (V_{DS} = 3V).

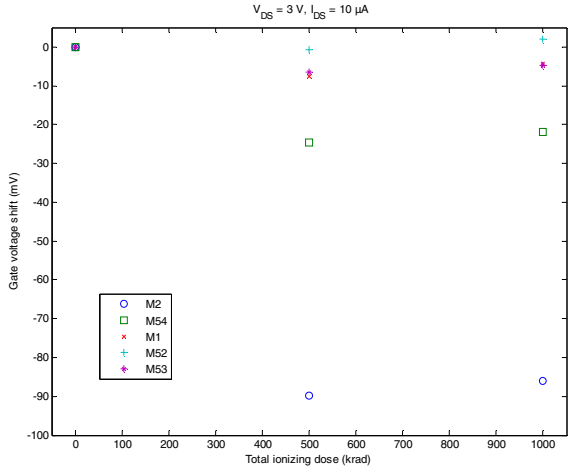

Fig. 6. V_{GS} shift (I_{DS} 10 µA) variation with TID for all NMOS transistor geometries (V_{DS} = 3V).

B. Noise Spectral Density Measurements

1) Experimental setup

Noise spectral density measurements were made at each irradiation step for each transistor type using a ×10 gain low noise amplifier (LNA) and an HP3585A spectrum analyser.

In the first phase of irradiations (unbiased) the output noise spectra were measured in a source follower configuration

(100 kΩ load) for 2 samples of each transistor at each dose. Measurements from this phase showed that the variability of noise spectra between different samples of the same device type was extremely large (and increased with reducing device geometry) and that any further investigation would require measurements from many samples of each transistor at each TID. No detailed analysis was therefore performed.

For the second phase irradiation (biased) noise spectra were acquired for 10 samples of each transistor type at each dose (0, 500 krad, 1 Mrad) to allow calculation of a mean noise spectrum for a given design at each irradiation step. The measurements were also improved in terms of bandwidth by using a wider bandwidth LNA and by connecting the transistors in a common source configuration to reduce parasitic capacitance. In this configuration it was also necessary to measure the gain to allow calculation of the gate referred noise spectral density at each frequency

Each noise spectrum was measured in the range from 100 Hz to 5 MHz for a drain current of 10 µA, which is typical for CIS use. The drain current was set by adjusting the gate-source voltage. The drain-source voltage was maintained at 3V (-3V for the PMOS transistors).

2) *Biased Irradiation Results*

The mean gate-referred noise spectra for all NMOS transistors are shown in Fig. 7. The noise density at a given frequency is seen to decrease with increasing channel area, as expected. Noise spectra for the smallest devices are indicative of random telegraph signal (RTS) behaviour whereas the larger devices exhibit 1/f dependence. Following irradiation to 500 krad the smallest transistor shows a clear increase in noise density across the spectrum but the trend following the second 500 krad is not as obvious. This increase appears to reduce as the channel area increases. For the largest transistor the effect of dose is not clear.

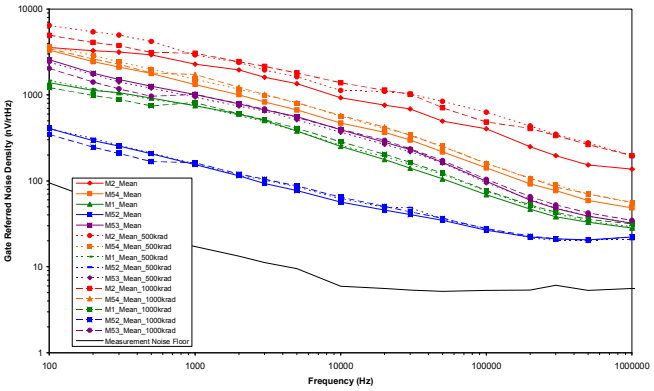

Fig. 7. Effect of TID on mean noise spectra for each NMOS transistor.

The mean gate-referred noise spectra for both PMOS transistors are shown in Fig. 8. As before spectra for the smallest device show RTS characteristics whereas the largest are 1/f dominated. Overall noise following irradiation is seen to increase for the small geometry device whereas the largest device is unchanged, within the measurement errors.

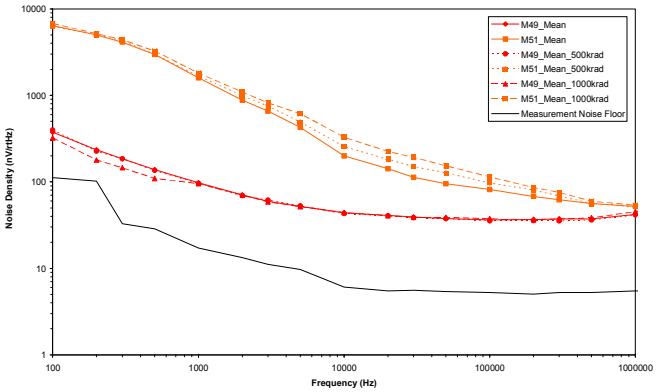

Fig. 8. Effect of TID on mean noise spectra for each PMOS transistor.

IV. Summary and Conclusions

There is considerable information in the literature relating to ionizing radiation effects on full-scale CIS devices [6][7][8], conversely there is relatively little information regarding effects on the individual transistors in the context of CMOS imaging devices [9][10].

This study has investigated the effects of ionising radiation on I-V and noise characteristics of individual transistors of various geometries. The key findings are that leakage current is significantly increased following irradiation to 500 krad and is more severe for small geometry devices. No further increase was found following irradiation to 1 Mrad as previously noted in [10]. PMOS I-V characteristics were relatively unchanged.

Noise spectral density measurements showed that noise in larger geometry devices is relatively unchanged following irradiation, whereas smaller geometry devices - which are dominated by RTS effects - show an increase. Similar results were observed for the PMOS devices.

The results demonstrate I-V characteristics can be significantly modified as a result of trapped charge build-up in the trench oxide. The resulting parasitic leakage currents could be problematic for optimal operation of CIS devices as transistors are often used as in-pixel switches, for example to reset the photodiode or access the pixel signal. Quantification of these leakage currents is important to determine if they are manageable through appropriate operation or if design changes need to be made, for example by using radiation-hard structures such as ring-gate transistors or PMOS transistors. Such a change would have implications for pixel design and overall sensitivity.

Acknowledgement

The authors would like to thank Andrew Pike and Jerome Pratlong at e2v for coordinating packaging of the Test Structures and providing guidance on operating parameters.

References

[1] O. Grasset et al, JUpiter ICy moons Explorer (JUICE): An ESA mission to orbit Ganymede and to characterise the Jupiter system, *Planetary and Space Science*, Volume 78, April 2013, Pages 1-21

[2] Hardy, T.; Murowinski, R.; Deen, M.J., "Charge transfer efficiency in proton damaged CCD's," *Nuclear Science, IEEE Transactions on* , vol.45, no.2, pp.154,163, Apr 1998

[3] Bedabrata Pain ; Bruce R. Hancock ; Thomas J. Cunningham ; Suresh Seshadri ; Chao Sun ; Pavani Pedadda ; Christopher J. Wrigley ; Robert C. Stirbl; Hardening CMOS imagers: radhard-by-design or radhard-by-foundry. Proc. SPIE 5167, January 12, 2004

[4] Fossum, E.R., "CMOS image sensors: electronic camera-on-a-chip," *Electron Devices, IEEE Transactions on*, vol.44, no.10, pp.1689,1698, Oct 1997.

[5] T. P. Ma; P. V. Dressendorfer, *Ionizing Radiation Effects in MOS Devices and Circuits,* USA, Wiley, 1989.

[6] Bogaerts, J.; Dierickx, B.; Meynants, G.; Uwaerts, D., "Total dose and displacement damage effects in a radiation-hardened CMOS APS," *Electron Devices, IEEE Transactions on* , vol.50, no.1, pp.84,90, Jan 2003

[7] Hopkinson, G.R.; Mohammadzadeh, A.; Visconti, A., "Radiation effects on a radiation-tolerant CMOS active pixel sensor," *Nuclear Science, IEEE Transactions on* , vol.51, no.5, pp.2753,2762, Oct. 2004..

[8] Cohen, M.; David, J-P, "Radiation-induced dark current in CMOS active pixel sensors," *Nuclear Science, IEEE Transactions on* , vol.47, no.6, pp.2485,2491, Dec 2000..

[9] Ratti, L.; Andreoli, C.; Gaioni, L.; Manghisoni, M.; Pozzati, E.; Re, V.; Traversi, G., "TID Effects in Deep N-Well CMOS Monolithic Active Pixel Sensors," *Nuclear Science, IEEE Transactions on* , vol.56, no.4, pp.2124,2131, Aug. 2009

[10] Gaillardin, M.; Goiffon, V.; Girard, S.; Martinez, M.; Magnan, P.; Paillet, P., "Enhanced Radiation-Induced Narrow Channel Effects in Commercial 0.18µm Bulk Technology," *Nuclear Science, IEEE Transactions on* , vol.58, no.6, pp.2807,2815, Dec. 2011